NLX Electrical Design Suggestions

Version 1.21

IMPORTANT INFORMATION AND DISCLAIMERS

1. INTEL CORPORATION (AND ANY CONTRIBUTOR) MAKES NO WARRANTIES WITH REGARD TO THIS NLX DOCUMENT AND IN PARTICULAR DOES NOT WARRANT OR REPRESENT THAT THIS DOCUMENT OR ANY PRODUCTS MADE IN CONFORMANCE WITH IT WILL WORK IN THE INTENDED MANNER. NOR DOES INTEL (OR ANY CONTRIBUTOR) ASSUME RESPONSIBILITY FOR ANY ERRORS THAT THE DOCUMENT MAY CONTAIN OR HAVE ANY LIABILITIES OR OBLIGATIONS FOR DAMAGES INCLUDING, BUT NOT LIMITED TO, SPECIAL, INCIDENTAL, INDIRECT, PUNITIVE, OR CONSEQUENTIAL DAMAGES WHETHER ARISING FROM OR IN CONNECTION WITH THE USE OF THIS DOCUMENT IN ANY WAY.

2. NO REPRESENTATIONS OR WARRANTIES ARE MADE THAT ANY PRODUCT BASED IN WHOLE OR IN PART ON THE DOCUMENT WILL BE FREE FROM DEFECTS OR SAFE FOR USE FOR ITS INTENDED PURPOSE. ANY PERSON MAKING, USING OR SELLING SUCH PRODUCT DOES SO AT HIS OR HER OWN RISK.

3. THE USER OF THIS DOCUMENT HEREBY EXPRESSLY ACKNOWLEDGES THAT THE DOCUMENT IS PROVIDED AS IS, AND THAT INTEL CORPORATION (AND ANY CONTRIBUTOR) MAKES NO REPRESENTATIONS, EXTENDS NO WARRANTIES OF ANY KIND, EITHER EXPRESS OR IMPLIED, ORAL OR WRITTEN, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTY OR REPRESENTATION THAT THE DOCUMENT OR ANY PRODUCT OR TECHNOLOGY UTILIZING THE DOCUMENT OR ANY SUBSET OF THE DOCUMENT WILL BE FREE FROM ANY CLAIMS OF INFRINGEMENT OF ANY INTELLECTUAL PROPERTY, INCLUDING PATENTS, COPYRIGHT AND TRADE SECRETS NOR DOES INTEL (OR ANY CONTRIBUTOR) ASSUME ANY OTHER RESPONSIBILITIES WHATSOEVER WITH RESPECT TO THE DOCUMENT OR SUCH PRODUCTS.

4. A LICENSE IS HEREBY GRANTED TO COPY AND REPRODUCE THIS DOCUMENT FOR ANY PURPOSE PROVIDED THIS “IMPORTANT INFORMATION AND DISCLAIMERS” SECTION (PARAGRAPHS 1-4) IS PROVIDED IN WHOLE. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY OTHER INTELLECTUAL PROPERTY RIGHTS IS GRANTED HEREIN.

Release 1.2, January 1998

† Other product and corporate names may be trademarks or registered trademarks of other companies and are used only for explanation and to the owners’ benefit, without intent to infringe.

Revision History

Revision 1.2 to 1.21	
Section 3.1.7.1:	Added figure to explain the USB termination.
Revision 1.1 to 1.2	
Section 2.8:	Added note and figure to describe the maximum tilt allowed for the 2×13 supplemental connector.
Section 3.1:	Added note and figure to describe the maximum tilt allowed for the 340-pin NLX connector.
Throughout:	Slight editorial changes for consistency and readibility.
Revision 1.0 to 1.1	
Section 1.2:	Clarified name and date of IEEE standard for a high performance serial bus. Clarified name of the Audio Codec '97 Component Specification.
Section 2.1.1:	Added footnote reference to the PCI Local Bus Specification.
Section 2.1.2	Added footnote about all terminations taking place on the riser unless otherwise stated in the specs.
Section 3.1.1:	Added text plus a table to list the PCI signal termination pullup requirement for each PCI signal.
Section 3.2:	Added or modified some PCI signal descriptions on the NLX Riser Checklist.

Contents

Figures

Tables

1. Overview

NLX is a new low profile motherboard form factor designed to improve upon today's low profile form factors, both mechanically and electrically. This document is intended to provide electrical design suggestions as a reference for OEMs to help them realize the benefits of the NLX form factor.

1.1 Definitions

The following list defines how terms are used in this document; they are not intended to be industry definitions.

AGP—Accelerated Graphics Port. Refers to the devices supporting 1.0 of the A.G.P. specification.

Bus Mastering—The ability for a PCI agent to function as an initiator in a PCI transactions. For this to be possible, the agent must have access to a REQ#/GNT# pair of the PCI arbiter.

End to End—A motherboard layout where the processor and DIMM memory are placed so that their ends are closest together (see Figure 2: Motherboard "End to End" Layout).

Face to Face—A motherboard layout where the processor and DIMM memory are placed so that their sides are closest together (see Figure 3: Motherboard "Face to Face" Layout).

I/O Slot—Either a PCI or ISA connector that supports an add-in card.

PCI Agent—Either a PCI device or add-in card.

Pulldown Resistor—A resistive element used to place an undriven signal in a logic low state.

Pullup Resistor—A resistive element used to place an undriven signal in a logic high state.

REQ#/GNT#—Refers to the PCI request and grant signals on the PCI bus. Each request signal has an associated grant signal.

Parallel Termination—The process of adding a resistive element between a signal and either power or ground sources.

Series Termination—The process of adding a resistive element in series with a signal to provide a means of reducing ringing and ensuring signal integrity.

Termination—The process of adding either series or parallel termination to a signal.

1.2 Related Documents

- *NLX Power Supply Recommendations*
- *PCI Local Bus Specification,* Revision 2.1
- *PCI Bus Power Management Interconnect (PCI-PM) Specification,* Revision 1.0
- *IEEE Standard for a High Performance Serial Bus* (#1394-1995)
- *Audio Codec '97 Component Specification,* Revision 1.03

2. NLX Motherboard to Riser Electrical Design

NLX improves upon existing low-profile form factors by placing the I/O riser on the side of the motherboard and thereby freeing up critical routing channels. However, this imposes certain challenges to some of the high speed buses and signals because the routing length becomes more of a concern. The following sections address some of the electrical issues that must be resolved in the interface between the motherboard and riser in NLX systems.

2.1 PCI Bus

Because the PCI bus is a high speed bus, special care is needed in routing this bus on NLX systems. The following are suggestions for routing the PCI bus on both the riser and motherboard.

2.1.1 PCI Simulation

As defined in the NLX specification, the PCI bus should be terminated on the riser[1]. This is determined to be optimal from PCI bus simulations. This section summarizes how the PCI bus was simulated in an NLX system. Figure 1 shows the riser card layout that was used in the simulation exercise. Figure 2 represents the topology for end to end layout, and Figure 3 for face to face layout. See the next section for the simulation results and recommendations.

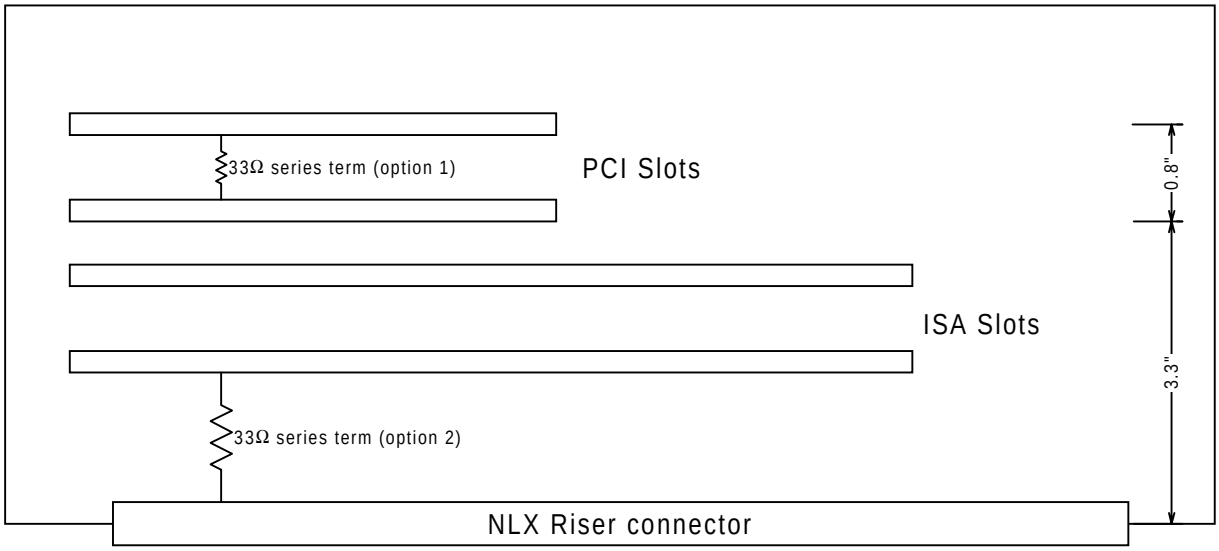


Figure 1: Riser Card Layout for Simulation Exercise

Note: Relevant distances for this card are as follows:
Longest routed signal from NLX riser edge connector to first PCI slot is 3.3".
Distance between ISA slots or between PCI slots is 0.8".
Distance between shared PCI-ISA slot is 0.5".

[1] Please refer to PCI Specification 2.1 for more detail about which type of termination to use (series or parallel).

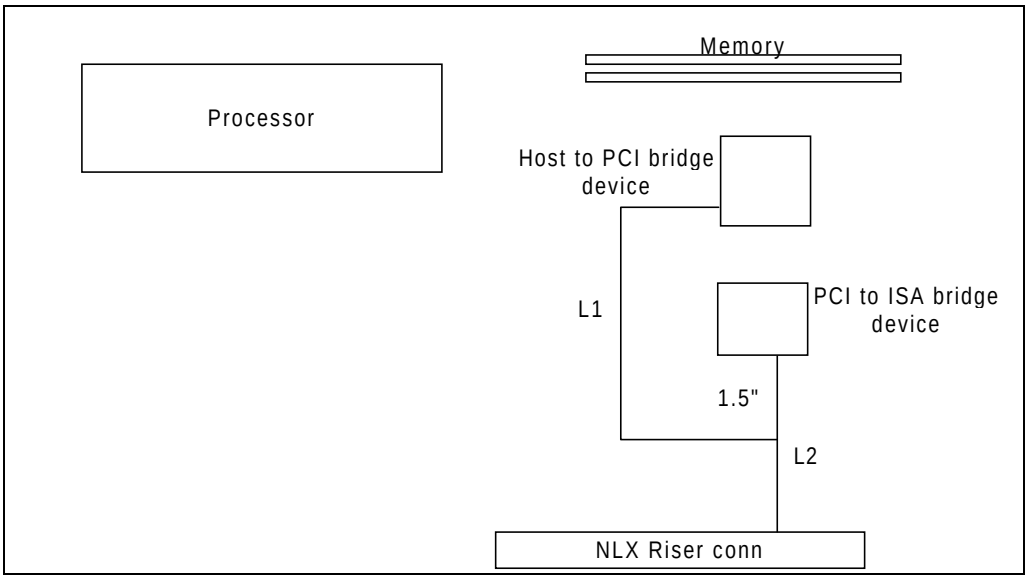


Figure 2: Motherboard "End to End" Layout

Note: For the exercise, the stub for the PCI-ISA bridge device is fixed at 1.5".

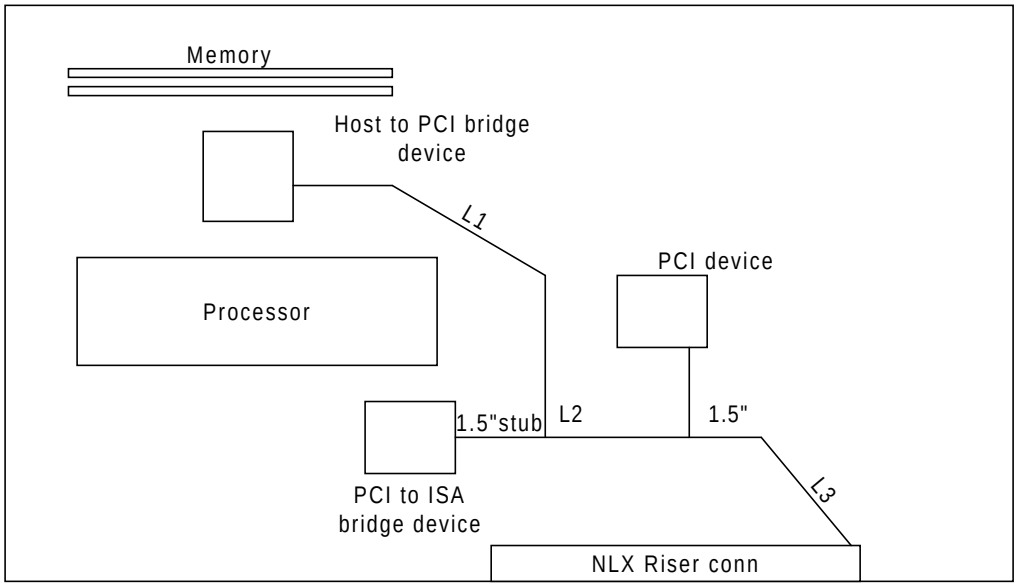


Figure 3: Motherboard "Face to Face" Layout

Note: For the exercise, the stubs for the PCI-ISA bridge device and PCI device are fixed at 1.5".

2.1.2 Simulation Results and Recommendations[2]

This section describes the results and recommendations based on the PCI simulation. The results presented are for a specific motherboard chipset and riser combination. To ensure proper PCI bus operation, motherboard and riser OEMs should perform their own independent simulations to help guide their choice and layout of components.

End to end layout (Figure 2): The results from the simulation show that with typical riser implementations, this layout cannot be achieved without termination. Without termination, the maximum line length for L1 in Figure 2 is 4.0", and the maximum line length for L2 is 1.5". Two reflections affect flight times. The initial incident reflection occurs between 7 and 10ns and causes as much as 2.0v of ring back. A second reflection occurs between 14 and 17ns, resulting in reflections up to 1.0 V. For most line lengths, the second reflection is close to the threshold of 0.8 V. The L1 and L2 line lengths are very sensitive to the second reflection, thus requiring the use of series termination.

- Series termination between the PCI slots is found to be effective (Figure 1, option 1). Simulations show that the maximum L1 length can be increased to 6.0" and L2 length to 1.5".
- For best results, use a 33 ohm series termination between the NLX riser connector and first ISA slot (Figure 1, option 2). With termination used, the signal quality improves dramatically, rarely crossing the threshold. The maximum line length L1 could be increased to 8.0" and the maximum L2 line length to 2.5".

Face to face layout (Figure 3): The results from the simulation show that with typical riser implementations, this layout cannot be achieved without termination. Without termination, the maximum line lengths of the PCI bus are 5.0" for L1, 2.0" for L2, and 1.0" for L3. L3 is the critical length, because trace lengths above 1.0" will result in flight time violations. Also, signal quality shows a large reflection on the rising edge dipping to 1.8v, and rising to 1.5v on the falling edge. This occurs when the PCI-ISA bridge device is driving the PCI bus.

- Series termination between the PCI slots is not found to be effective for line length L3 (Figure 1, option 1). Even with termination between the PCI slots, the line length L3 is still held to 1.0", although flight times improved.
- For best results, use a 33 ohm series termination between the NLX riser connector and first ISA slot (Figure 1, option 2). With termination used, the maximum line length L3 could be increased to 4.0" with L1 at 7" and L2 at 2". Another alternative exists with L1 at 7", L2 at 3", and L3 at 3".

Simulations also show that the 3.3" of trace to the first PCI slot plus the additional 0.8" to the second slot contribute to the settling time. In most cases, using a load card in either PCI slot for both layouts does not have a significant effect on settling times.

The recommendation from the PCI bus simulation exercises is that the riser card implement 33 ohm series termination of the bus between the connector and the first connector, whether it be ISA or PCI. This implementation results in significant gains in both motherboard layout options.

---

[2] Note that **all** terminations take place on the riser unless otherwise stated in the specifications.

2.1.3 PCI REQ#/GNT# Implementation

The only exception to PCI bus termination on the riser is in the REQ#/GNT# pairs. A possible problem exists when there are bus-mastering motherboard devices as well as when the motherboard chipset does not support as many bus-mastering pairs as there are available on the riser. If the REQ#/GNT# pair of the motherboard device is routed to the riser, a contention problem will exist when a bus-mastering device is installed in the I/O slot that has the same REQ#/GNT# pair. To alleviate this contention, when you have a motherboard device that requires a REQ#/GNT# pair, terminate these signals on the motherboard at the device and do not route them to the riser.

Also, if the riser has support for multiple PCI slots, it cannot be sure that clocks and/or REQ#/GNT# pairs go to all of the slots. To alleviate this problem, motherboard manufacturers should clearly define in their documentation how many PCI bus-mastering add-in cards as well as nonbus-mastering cards will be supported. If possible, the motherboard should route 33 MHz clocks to all five PCI clock signals on the riser connector so that the motherboard will support nonbus-mastering cards in all possible riser slots. If the motherboard is incapable of supporting all five PCI clocks, PCICLK0 should be the first one supported, PCICLK1 the second, and so forth.

2.1.4 64-bit PCI

OEMs designing riser cards should take into account that add-in cards supporting the 64-bit extension to the PCI bus may be used in the 32-bit connectors. Therefore, special attention should be given to ensure that no components are placed on the risers in areas that may conflict with the 64-bit extension of these cards.

2.1.5 IDSEL Assignment

Table A.1 of the NLX motherboard specification defines the recommended IDSEL assignments for the I/O slots on the riser. The motherboard should begin assigning IDSEL signals from the lower address lines. This has implications for the system BIOS in terms of which PCI devices are initialized first within a system. For example, if the system BIOS scans downward in the initialization routine (i.e., AD31 to AD11), the devices on the add-in board on the riser will be initialized before the motherboard devices. The opposite is true if the BIOS scans upward: the BIOS will find the motherboard devices before the devices on the add-in boards.

2.1.6 PCI_PM#

The exception to PCI termination is the PCI power management signal. Because power management is driven by motherboard circuitry, which in turn may be at various power wells, the motherboard is responsible for pulling the signal up to the motherboard-defined power level.

2.2 ISA Signals

All ISA signals that require termination should have the resistor located on the motherboard. This prevents an unterminated ISA bus when a motherboard is mated with a riser that does not have ISA connectors.

2.3 IDE Signals

All signals requiring parallel termination except IDEx_DASP should be terminated (if required) on the motherboard. IDEx_DASP should be terminated on the riser card. Preliminary simulation activities indicate that for ATA-33 support, the cable length should not exceed 12 inches. This minimizes the amount of crosstalk that occurs on 18-inch cables at these speeds. Table 1 shows the IDE signals as they relate to the IDE connector and NLX connector.

Table 1: IDE Signals

Primary IDE header	Signal name	Riser pin #	Primary IDE header	Signal name	Riser pin#
1	IDEA_RESET#	A103	2	GND	-
3	IDEA_DD7	B103	4	IDEA_DD8	A102
5	IDEA_DD6	B104	6	IDEA_DD9	A104
7	IDEA_DD5	B105	8	IDEA_DD10	A107
9	IDEA_DD4	A106	10	IDEA_DD11	B106
11	IDEA_DD3	A108	12	IDEA_DD12	B107
13	IDEA_DD2	B110	14	IDEA_DD13	A109
15	IDEA_DD1	A110	16	IDEA_DD14	B109
17	IDEA_DD0	B111	18	IDEA_DD15	B112
19	GND	-	20	KEY	-
21	IDEA_DMARQ	A113	22	GND	-
23	IDEA_DIOW#	A112	24	GND	-
25	IDEA_DIOR#	B113	26	GND	-
27	IDEA_IORDY	A114	28	IDEA_CSEL	B114
29	IDEA_DMACK#	A115	30	GND	-
31	IDEA_INTRQ	B115	32	IDEA_RESRV	-
33	IDEA_DA1	B117	34	RESERVED	-
35	IDEA_DA0	B118	36	IDEA_DA2	A117
37	IDEA_CS0#	A118	38	IDEA_CS1#	B119
39	IDEA_DASP#	A120	40	GND	-

Table 1: IDE Signals, continued

Secondary IDE header	Signal name	Riser pin #	Secondary IDE header	Signal name	Riser pin#
1	IDEB_RESET#	A121	2	GND	-
3	IDEB_DD7	B121	4	IDEB_DD8	B120
5	IDEB_DD6	A123	6	IDEB_DD9	A122
7	IDEB_DD5	A124	8	IDEB_DD10	B123
9	IDEB_DD4	B125	10	IDEB_DD11	A125
11	IDEB_DD3	B126	12	IDEB_DD12	A126
13	IDEB_DD2	A128	14	IDEB_DD13	B127
15	IDEB_DD1	B129	16	IDEB_DD14	B128
17	IDEB_DD0	B130	18	IDEB_DD15	A129
19	GND	-	20	KEY	-
21	IDEB_DMARQ	A131	22	GND	-
23	IDEB_DIOW#	A130	24	GND	-
25	IDEB_DIOR#	B131	26	GND	-
27	IDEB_IORDY	A132	28	IDEB_CSEL	B132
29	IDEB_DMACK#	A134	30	GND	-
31	IDEB_INTRQ	B133	32	IDEB_RESRV	-
33	IDEB_DA1	B134	34	RESERVED	-
35	IDEB_DA0	A136	36	IDEB_DA2	B135
37	IDEB_CS0#	A137	38	IDEB_CS1#	B136
39	IDEB_DASP#	B137	40	GND	-

2.4 Floppy Signals

All signals requiring termination should be terminated on the riser. Table 2 shows the floppy signals as they relate to the floppy connector and the NLX connector.

Table 2: Floppy Signals

FDC header	Signal name	Riser pin #	FDC header	Signal name	Riser pin#
1	DRV2#	A138	2	DENSEL	A141
3	GND	-	4	FLPY_RSVD	-
5	KEY	-	6	DRATE0	B139
7	GND	-	8	INDX#	A143
9	GND	-	10	FDME0#	A142
11	GND	-	12	FDS1#	B140
13	GND	-	14	FDS0#	B141
15	GND	-	16	FDME1#	A144
17	MSEN1	B143	18	DIR#	B142
19	GND	-	20	STEP#	A147
21	GND	-	22	WRDATA#	B145
23	GND	-	24	WE#	A146
25	GND	-	26	TRK0#	B146
27	MSEN0	B147	28	WP#	A148
29	GND	-	30	RDDATA#	B148
31	GND	-	32	HDSEL#	A149
33	GND	-	34	DSKCHG#	B149

2.5 Power Signals

These signals provide the interface from the motherboard to the power supply connector on the riser.

2.5.1 1394PWR

Please refer to the IEEE standard 1394-1995 for 1394 power implementation guidelines. This signal is meant to provide a segregated power source that IEEE 1394 devices can use. The power supplied through this pin should be used only to provide bus power through the 1394 connector.

2.5.2 1394GND

This signal is meant to provide an isolated return for IEEE 1394 signals.

2.5.3 PWR_OK

This signal is asserted high by the power supply to indicate that +5 VDC and +3.3VDC outputs are above the voltage thresholds specified by the power supply. The logic designer can assume that when this signal is asserted, the power supply will deliver the continuous energy specified by the

power supply. Many power supplies have limited drive capability, so the designer is encouraged to consult the power supply documentation and provide bulk capacitors where needed.

2.5.4 PS_ON#

This signal is driven by circuitry on the motherboard to toggle the power state of the power supply. This is an open drain signal.

2.5.5 SOFT_ON/OFF#

This signal is required by the front panel of the system to allow the user to turn on or off the power rails of the power supply. The signal is driven down to the motherboard, where circuitry will detect the signal and subsequently use the PS_ON# signal to toggle the power state of the system. The power supply should provide the pullup resistor to +5 VSB. The motherboard provides any required debounce circuitry and an appropriate pullup resistor to a TTL level

2.5.6 5VSB

The 5V Stand By signal is capable of carrying 1.5 A, although typical power supplies can only source a fraction of that. Refer to the NLX power supply recommendations document for more details.

2.6 Audio Signals

Audio on the standard 340-pin connector has been limited to support of the PC speaker. The supplemental connector is used to route the traditional audio signals between the motherboard and riser. Refer to section 2.8.1 for details on routing traditional audio on the riser.

2.6.1 PCSPKR_L/R

These signals are meant to drive an 8 ohm speaker on the riser. In systems that support a mono PC speaker, the left signal must be used.

2.7 Miscellaneous and Front Panel Signals

The following subsections define in more detail the miscellaneous and front panel signals of the NLX specification.

2.7.1 SER_IRQ

This signal is used to implement the serialized IRQ requirements set forth in the Serialized IRQ Support for PCI Systems document. Refer to the Serialized IRQ Support for PCI Systems document for more details.

2.7.2 RSVD

These signals are reserved for future implementations and should not be used under any circumstances.

2.7.3 PWRLED#

This signal is routed from the motherboard to the riser to drive an LED that indicates that the system is active. The signal is active low, indicating that power is active in the system. This signal in the inactive or high state indicates that the system is in a sleep state. Refer to section 3.1.7.6 for examples on how this LED can be implemented on the riser. The exact implementation is up to the riser/system designer. The riser should have a current limiting resistor.

2.7.4 LAN_LED#

This signal is routed to the riser to provide control for an LED that will indicate that LAN activity is occurring. The riser should have a current limiting resistor.

2.7.5 FP_SLEEP

This signal is routed from the riser to the motherboard and provides request for the system to enter a power-saving mode. One implementation is to use this signal in conjunction with power management software and hardware to place the system in a sleep state. This functionality is typically implemented using a momentary contact switch on the front panel. The motherboard should have any required debounce and a weak pulldown resistor.

2.7.6 FP_RST#

This signal corresponds to a front panel reset signal to the motherboard. This should be implemented using a momentary contact switch on the front panel. When the switch makes contact, the signal is grounded. The motherboard should have any required debounce pullup resistor.

2.7.7 MDM_WAKE#

This signal provides the capability for a modem implemented on the riser routed to request the system to wake up from a power-managed state. Riser cards should support a header that allows cables from I/O cards.

2.7.8 LAN_WAKE

This signal provides the capability for a LAN implementation on the riser to request the system to wake up from a power-managed state. This signal should stay low when power is applied to the system so that system logic does not enter nondefined states. Riser cards should support a header that allows cables from I/O cards.

2.7.9 Infrared Signals

These five signals implement the IR interface as defined in the industry. Refer to the industry specification as a reference on how this interface should be implemented. The termination of these signals should be done at the controller.

2.7.10 MSG_WTNG_LED#

This signal provides the interface to the riser to indicate that the system has received a telephone message. Refer to the riser and motherboard design sections for possible signal implementations.

2.7.11 USB Data

The motherboard should contain any required series termination on the data lines, and the termination should be placed as close as possible to the USB controller. The pulldown resistor should also be located on the motherboard; however, the placement is not critical.

2.7.12 USB_OCx#

In typical applications a thermistor will be located near the USB connector. In this implementation the thermistor is responsible for providing the pullup of this signal. If a riser does not implement a USB port, the riser should provide a strong pullup resistor on this signal.

2.7.13 FAN_TACH

These signals run from 0V to a maximum of +12V. The motherboard must provide any voltage conversion for 5V or 3.3V devices.

2.7.14 FAN_CTL

This signal is used to control fan RPM rate. The exact speed of the fans controlled by this signal will depend on the implementation. Because of this, the system designer should ensure that all of the system acoustics and cooling requirements are met when this signal is set for maximum fan speeds. The signal sets the fans to maximum speed when the voltage potential on FAN_CTL is 10.5 volts or greater. This signal sets the fans to minimum speed (off) when this signal is 1 volt or less. Fan speeds in between can be achieved by setting the voltage potential of this pin between 1 and +10.5 volts. Figure 4 shows a block diagram of the fan control circuitry. The maximum current supplied by this signal is 50mA and is not meant to drive fans directly. Internal Power Supply fan driving circuitry has been allotted 20mA of the available 50mA from this signal. Remaining 30mA may be used for circuitry on the riser or motherboard to drive other fans in the system. The FAN_CTL signal should be pulled up with a 10K (minimum) pullup resistor to +12 volts on the riser card. This will ensure that as a default the fan control signal will be set to full speed.

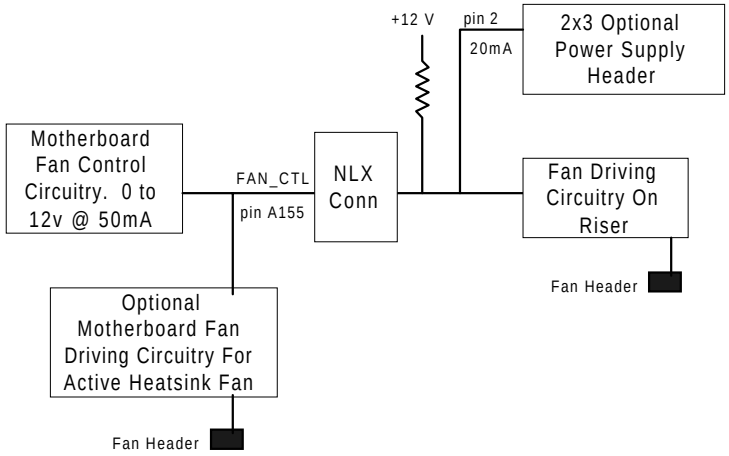


Figure 4: Block Diagram of Fan Control Circuitry

2.7.15 TAMP_DET#

Current implementations of this signal have a switch on the riser, powered from either VBAT or 5VSB, that is activated when the chassis cover is removed. Once activated, the motherboard can do one of several things, such as turning the power off if the system power is on. This would prevent someone from trying to remove the motherboard while the system is in a power-managed state.

- Switch powered from VBAT: The advantage is that you can detect intrusion even if the system has the power cord removed. The disadvantage is that you adversely affect the battery life of your system.
- Switch powered from 5VSB: The advantage is that you do not adversely affect your system battery life, and the system will detect intrusion in all powered states. The disadvantage is that the intrusion detect can be avoided by pulling the power cord from the system.

2.7.16 VBAT

This signal provides battery voltage to riser card devices.

2.7.17 SDA/SCL

This is a serial data bus. A possible implementation is an interface to a serial EEPROM on the riser. This would allow a motherboard to possibly query the riser to determine what if any active devices exist on the riser. The NLX specification has reserved binary address 1010111 for possible future configuration implementations.

2.8 Supplemental Connector

The NLX supplemental connector is defined to address some of the analog and digital audio signals as well as other miscellaneous signals that are required in systems. These signals are defined sufficiently in the specification.

NOTE

For the supplemental connector, the maximum allowed connector tilt is 0.010 inches from the plane of the riser card for both the short and long axis. Excessive tilts could cause board insertion difficulties and damages. See Figure 5.

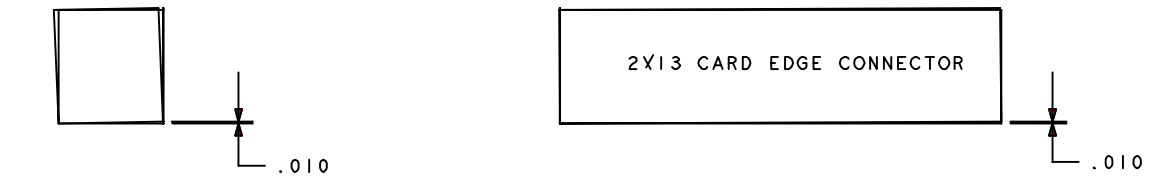


Figure 5: Connector Tilts for 2x13 Connector

2.8.1 Implementing Audio on NLX Platforms

Implementing audio in the computer has always been challenging because of the analog signals that must be routed. In NLX systems, if audio jacks are present on the front panel, then the optimum solution would be to use the supplemental connector to interface motherboard audio circuitry with the riser's audio jacks. In implementing audio jacks, the riser could either extend all the way to the front panel or cable up to the front panel. In either case, audio traces from the 2×13 supplemental connector need to be routed carefully to reduce noise from nearby digital signals. To avoid digital signals, the analog traces should be routed along the top edge of the riser. To further reduce the effects of nearby digital signals, a guard band tied to ground should be routed between the audio signals and the digital signals (Figure 6). Because the impedance will be high for the return path that is directly under the audio traces, the returning signals would normally use the ground pins of the 340-pin connector as a return path. For this reason the portion of the ground plane under the audio signals and circuitry should be isolated. This isolated ground should be tied back to the digital ground near the 2×13 auxiliary connector. As is always the case, stitching ferrites may be needed if EMI becomes a problem.

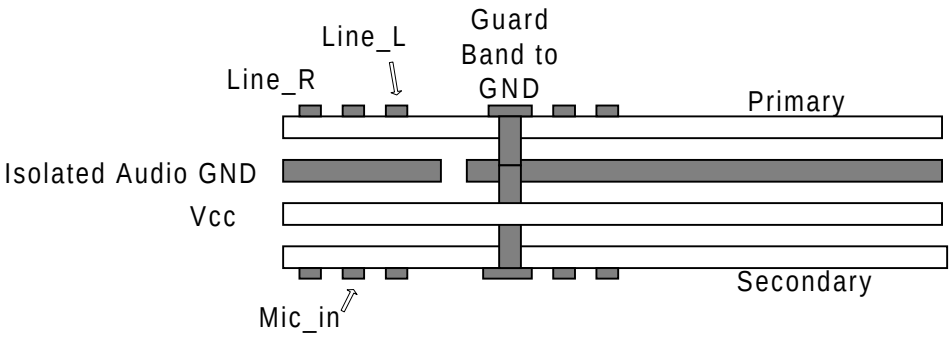


Figure 6: Example of Routing Audio on Riser

2.8.2 AC 97 Signals

These signals implement the five-signal AC 97 bus as defined in the *Audio Codec '97 Component Specification*.

2.8.3 SMI#

This is the standard open drain system management interrupt. The motherboard is responsible for the pullup resistor.

3. NLX Riser Design Suggestions

The following sections address the design issues that are specific to NLX Riser design.

3.1 NLX Connector Design

This section discusses the riser-specific issues of integrating the 340-pin NLX connector in riser designs.

NOTE

For the 340-pin connector, the maximum allowed connector tilt is 0.010 inches from the plane of the riser card for both the short and long axis. Excessive tilts could cause board insertion difficulties and damages. See Figure 7.

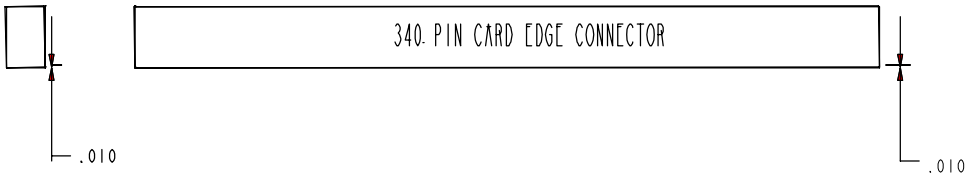


Figure 7: Connector Tilts for 340-pin Connector

3.1.1 PCI Bus Design

Simulation results show that to ensure the integrity of the PCI bus, the riser should provide 33 ohm series termination placed as close as possible to the 340-pin connector on the riser. Take great care in routing the PCI bus, and keep line lengths under 4.5″. Refer to section 2.1 for the complete simulation results.

Riser card designers should carefully consider which PCI I/O slot is assigned slot 1 resources. Slot 1 should be assigned the REQ0#/GNT0# pair and therefore is certain to support bus-mastering cards. As an example, in Figure 8 the slots are numbered so that slot 1 is the shared slot. If two ISA cards are required, the riser card designer might want to consider alternatives that allow the PCI slot 1 to be a nonshared slot.

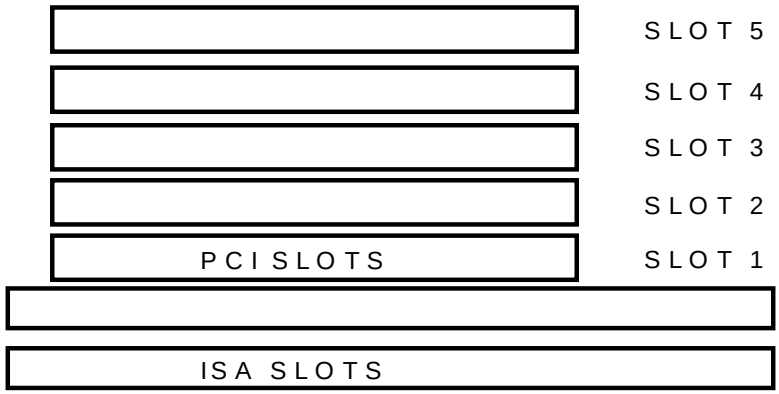


Figure 8: PCI and ISA Slot Configuration

Table 3 lists the PCI signal termination pullups. All pullups listed in the table should be implemented. For resistor values, refer to section 4.3.3 of the *PCI Local Bus Specification*, revision 2.1.

Table 3: PCI Signal Termination Pullup

Signal name	Pullup	On riser	On motherboard
PCI_PM#	Yes		X
FRAME#	Yes	X	
TRDY#	Yes	X	
IRDY#	Yes	X	
DEVSEL#	Yes	X	
STOP#	Yes	X	
SERR#	Yes	X	
PERR#	Yes	X	
LOCK#	Yes	X	
INTx#	Yes	X	
REQ64#	Yes	X	
ACK#64	Yes	X	
SBO#	Yes	X	
SDONE	Yes	X	

Note: All PCI siganls should have series resistors except unused REQ#/GNT# pairs, unused REQ64#/ACK64#, IDESEL, and CLK. These resistors should be placed close to the 340-pin NLX connector.

3.1.2 ISA Bus Design

Because all terminating resistors are on the motherboard, nothing specific should be done on the riser other than standard routing practices.

3.1.3 IDE Bus Design

All terminating resistors except those needed for IDEA_DSP and IDEB_DSP are on the motherboard. The pullup resistor to VCC for the above signals should be greater than 1K ohm. No special care is needed other than standard routing practices.

3.1.4 Floppy Bus Design

The pullup resistors required for the active low floppy signals are required to be on the riser. The value of these resistors should be greater than 1K ohm. No special care is needed other than standard routing practices.

3.1.5 Riser Power Design

- VCC and VCC3—The appropriate number of bulk and decoupling capacitors is required to adequately support system requirements. The bulk capacitors should be low in ESR and 22 uF or greater, and the number needed is system-specific. The bulk capacitors should be placed evenly throughout the pins on the connector. The decoupling capacitors should be in the range of 0.1 uF and placed judiciously around the NLX and power connectors. Also, there should be an adequate number of stitching capacitors linking the VCC and VCC3 power planes.
- +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.
- PS_ON#—This signal should be routed to the power connector and the 340-pin connector to allow the motherboard the ability to cycle power in the system. No other special care should be needed.
- SOFT_ON/OFF#—If implemented as a front panel control signal, route to the NLX connector. No other special care should be needed.
- PWROK—Route to the NLX connector and power supply connector. No other special care should be needed.

3.1.6 Riser PC Speaker Support

A typical chassis will support a mono speaker. In this case the PC_SPKR_LFT signal will need to be routed to an appropriate stake header, or to a speaker on the riser.

3.1.7 Miscellaneous and Front Panel Signal Design

Figure 9 shows an example of how a riser might implement support for the miscellaneous and front panel signals. This is a simple 100 mil header that allows a flexible implementation of cabling all signals to chassis-specific implementations. The alternative to supporting these signals is to define the riser to the specific chassis form and function. The specific function of these signals is described in Section 2.7. The miscellaneous and front panel signals that require more design considerations are described below.

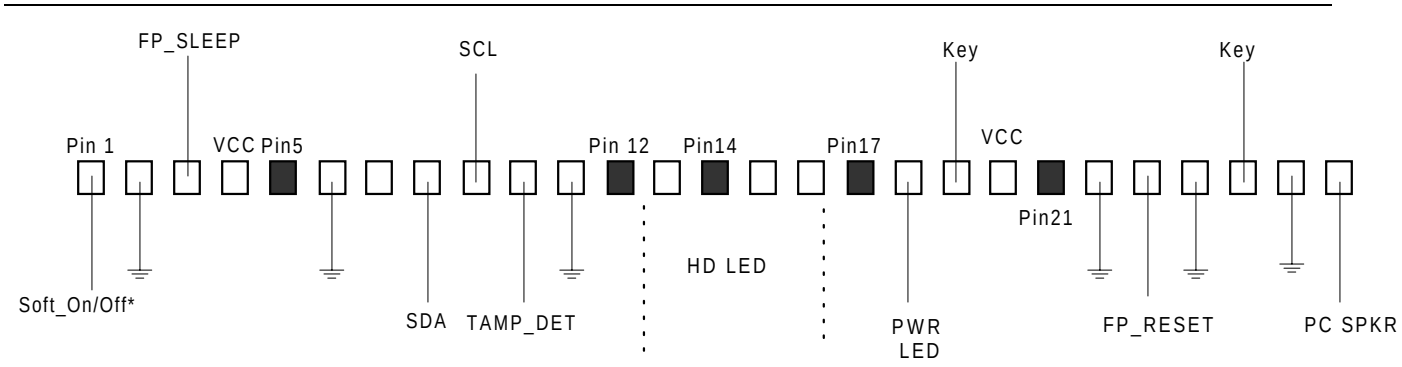


Figure 9: Miscellaneous and Front Panel Header

3.1.7.1 USB Riser Design

Because USB is a high speed serial bus, it offers some design challenges in supporting a front panel implementation. One implementation would be to carefully route the bus to a stake header and then cable to the front panel. Great care should be taken to address signal integrity and EMI issues. A possible implementation of supporting a USB header is shown in Figure 10.

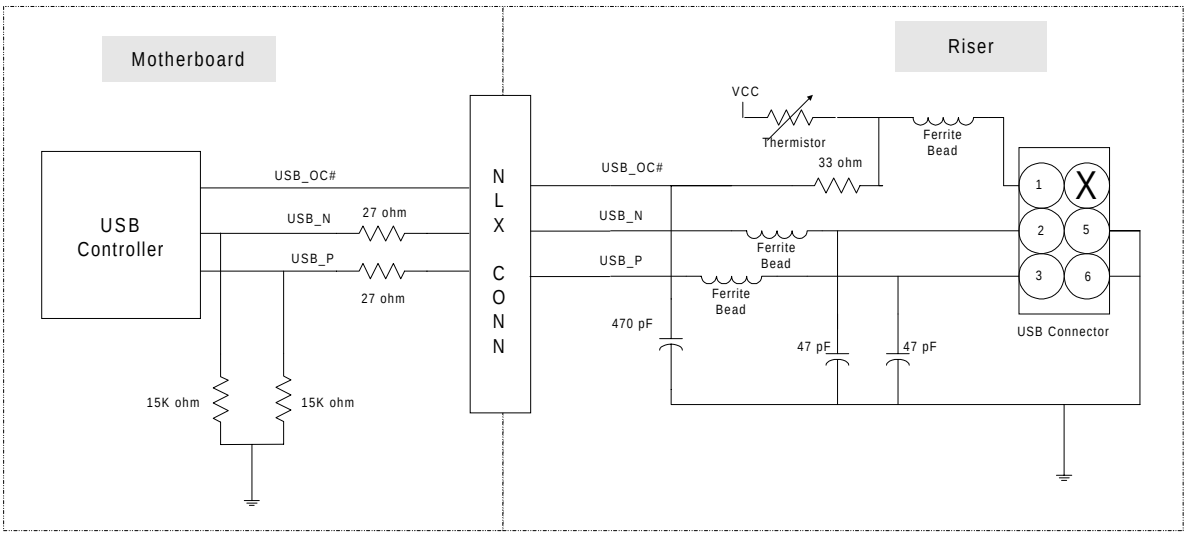


Figure 10: Possible USB Riser Implementation

Note that the thermistor is required to support overcurrent protection. The riser designer needs to implement protection from overcurrent conditions. Another possible implementation is to design the riser for a specific chassis form and function so that a USB connector could be placed directly on the riser PCB.

3.1.7.2 Infrared Riser Design

To support front panel infrared, the riser designer can route the bus to a stake header or, in chassis-specific implementations, to an IR connector on the PCB. A possible implementation of supporting an IR header is shown in Figure 11.

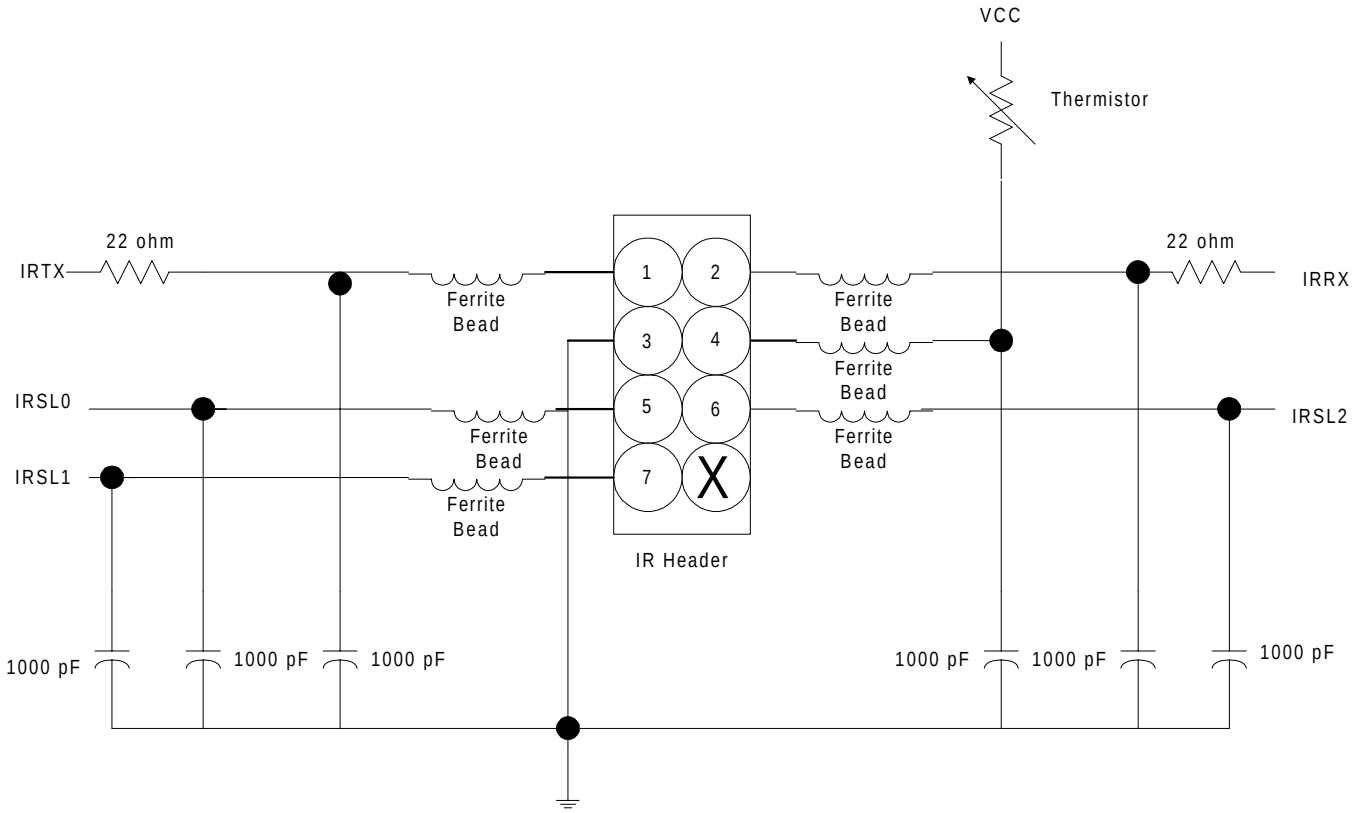


Figure 11: Possible IR Riser Implementation

3.1.7.3 Modem Wake

To support the ability to have an add-in modem wake up the system from a sleep state, a standard stake header will be required on the riser. This header will need to have 5VSB so that power to the modem is supplied while the system is asleep. A possible implementation is to combine this header with the tamper detect jumper; see definition in Table 4.

3.1.7.4 Tamper Detect Design

To help prevent the removal of the motherboard with the power on, chassis intrusion circuitry may be used to warn the user when the chassis cover is removed. An intrusion switch can be mounted near the top rear edge of the riser card to inform the user if the top of chassis is removed. This can be bypassed by depopulating the tamper detect enable jumper on the standard stake header defined in Table 4. The tamper detect support is defined in Figure 9.

A possible implementation could be if the cover is removed, the onboard speaker immediately starts beeping. The speaker will continue to beep until the lid is replaced, the tamper enable jumper is removed, or the system is unplugged (removing power from 5VSB). If the system is in a sleep mode when the lid is removed, the onboard speaker will again immediately start beeping.

Table 4: Tamper Detect and Modem Wake Header Definition

Pin #	Name
1	NC
2	GND
3	MDM-WAKE#
4	KEY
5	5VSB
6	KEY
7	TAMP_DET_ENABLE*
8	TAMP_DET_ENABLE

3.1.7.5 Fan Control

Circuitry similar to that shown in Figure 12 may be used to drive the fan on the riser. The voltage across the fan will be either 10.6 volts or 7.3 volts, depending on the output of the comparator, which in turn depends on whether the (-) input is above or below 9 volts. Decoupling caps should be used on this signal to minimize noise on the line.

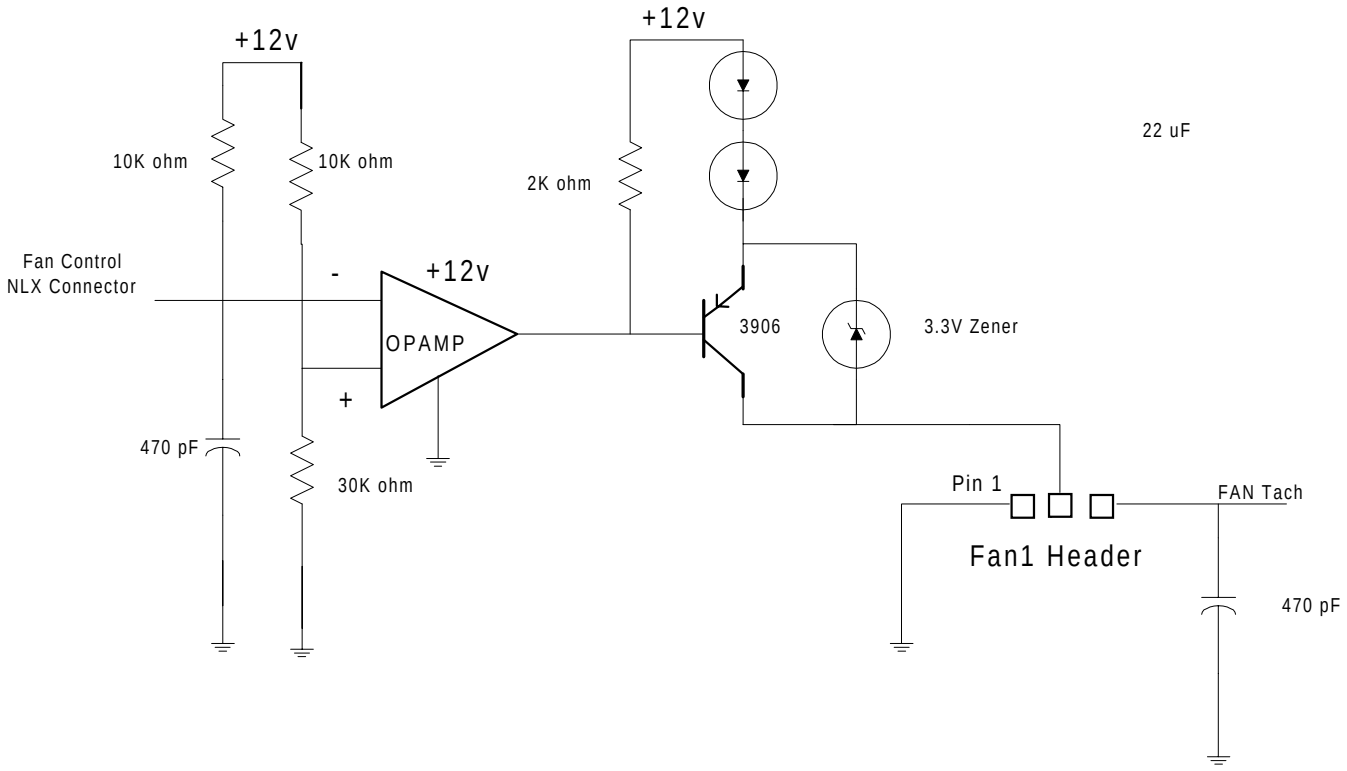
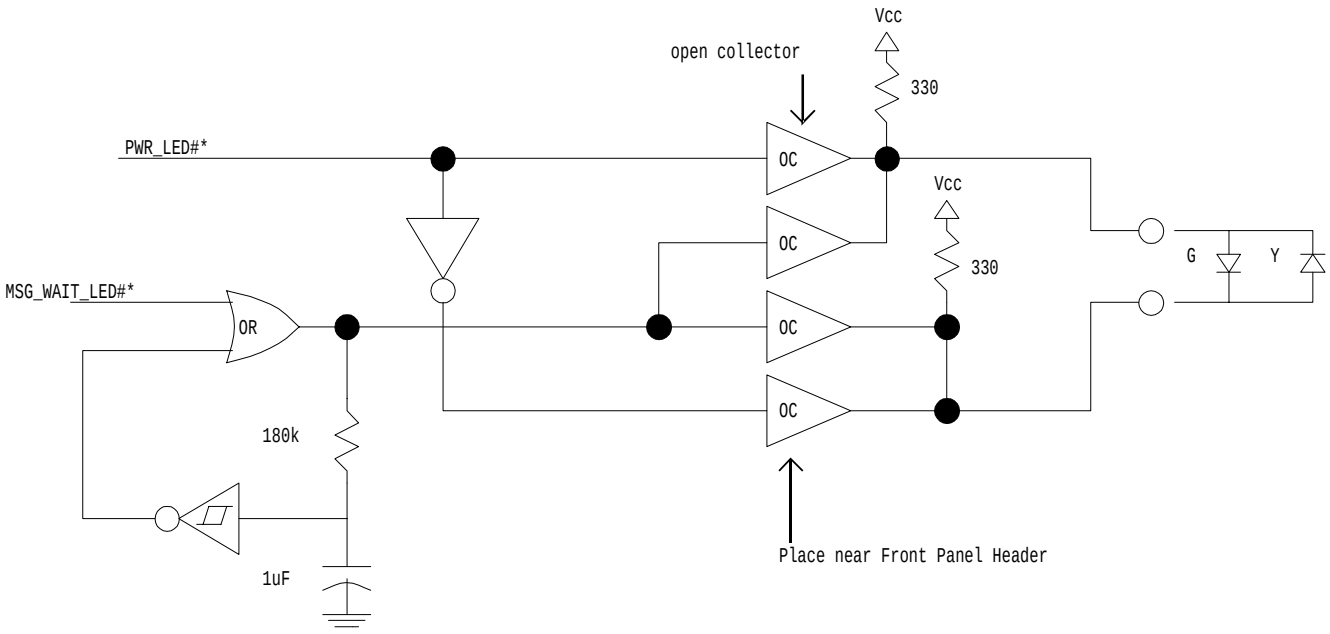


Figure 12: Riser Fan Control Circuitry

3.1.7.6 LED Support

The number of LEDs supported will be a function of the riser card and chassis combination. At a minimum the system should indicate to the user when the system is on, when the system is off, HDD activity, and optionally when there is a message waiting or LAN activity. In Figure 13, a configuration is shown whereby a dual color LED along with blink circuitry is used to define either the power-on state (green dual LED), the sleep state (yellow dual LED), and whether a message is waiting (blinking dual LED). In another implementation, the message-waiting blink could be a dedicated LED instead of the dual color LED.



INPUTS		OUTPUT STATES	MEANING
PWR_LED#*	MSG_WAIT_LED#		
OFF	OFF	OFF	OFF
1	1	Green LED On	ON
1	0	Green LED Blinks	ON/message
0	1	Yellow LED On	SLEEP
0	0	Yellow LED Blinks	SLEEP/message

Figure 13: Possible Riser LED Implementation

3.1.8 Supplemental Connector Design

Although support for the supplemental connector is optional, implementing the support will provide a robust solution that will eliminate any cables required to support audio. Refer to section 2.8.1 for details on routing audio signals on PCBs. The following sections deal with the issues of the supplemental connector that were not dealt with in section 2.8.

3.1.8.1 Audio Connectors

To support the ability to not have audio cables on the motherboard and possibly front panel audio jacks, it is suggested that, at a minimum, the riser implements a header whereby the microphone in, line out, and CD Audio in signals are supported. Because CD Audio already has a 1×4 ATAPI header defined, an additional header will need to be defined to support the additional signals required. A possible implementation is to define a standard 2×5 stake header with the audio signals defined as shown in Table 5.

Table 5: Audio Connector Definition

Pin #	Name	Pin #	Name
1	MIC_IN	6	LINE_OUT_LFT
2	KEY	7	FP_MIC_EN
3	+12V	8	FP_SPKR_EN
4	LINE_OUT_RT	9	-12V
5	AGND	10	GND

3.1.8.2 Telephony Support

To support telephony applications, a header is defined that provides the interface to add-in modem cards. A microphone input to the card (MODEM_MIC) and a mono output from the card (MODEM_SPKR) are required on the header. A typical telephony header is a 1×4 stake header that has pin 1 defined as the MODEM_SPKR, pins 2 and 3 as ground, and pin 4 as the MODEM_MIC.

To avoid possible contention and signal integrity issues, if the riser has microphone in and line out support and these signals are routed to a telephony header, then the signals from the header should not be routed to the supplemental connector. In this case an additional telephony header should be used to support the audio jacks that may reside on the motherboard. If the riser does not support microphone in and line out, then a header should still be supported with the signals routed to the supplemental connector.

3.2 NLX Riser Checklist

This section provides an informal checklist of suggestions about the riser electrical design. The checklist is meant for reference only and is not intended to be comprehensive. Figure 14 shows an example of a riser card.

NOTE

It is strongly recommended that the NLX specification be reviewed in sufficient detail that the designer is confident the design complies with the specification.

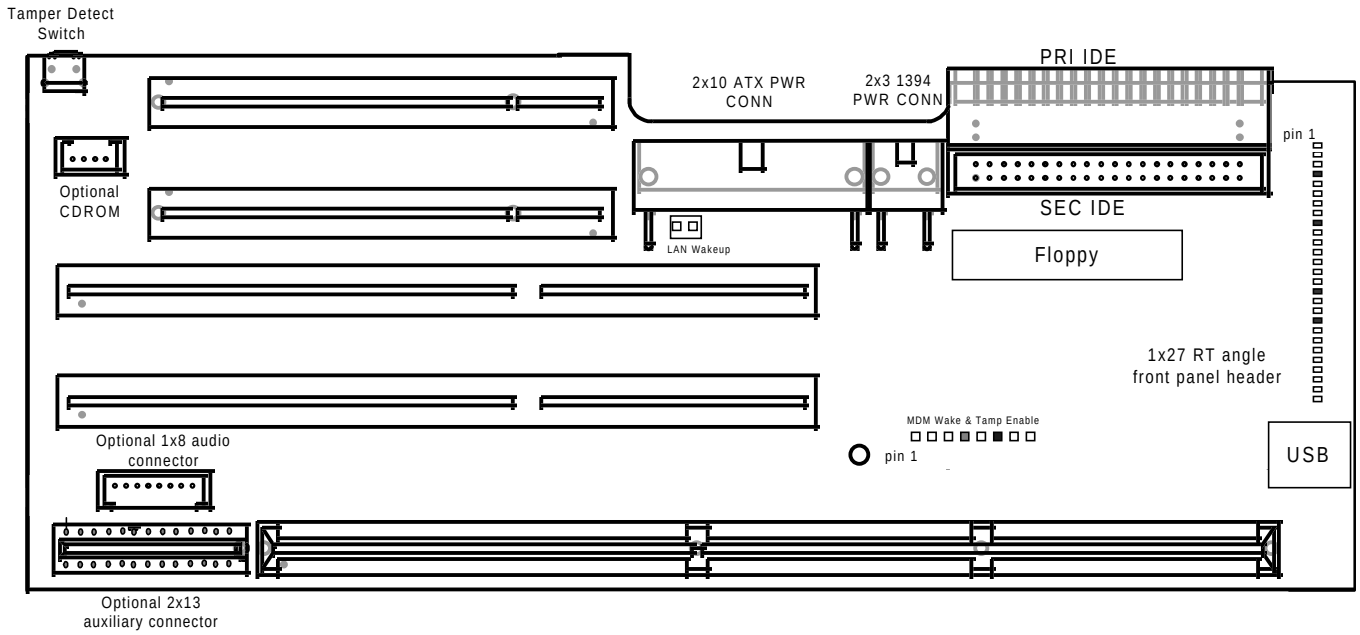


Figure 14: Riser Card Example

Riser Mechanical/Placement Requirements

- Ensure the integrity of the tilt and coplanarity of the supplemental and 340-pin connector.
- Ensure that add-in cards can be removed without hitting chassis features.
- Ensure that cables are easily accessible.
- If a tamper detect switch is implemented, ensure the integrity of the switch with the chassis cover on and off.
- Ensure that there are no violations of the keep-out zones on the sides of the 340-pin connector.

Riser NLX Card Edge Signal Issues

— Ensure that the 1mm pitch connector setup is as listed in Tables 4.8-4.11 in the NLX Motherboard Specification, with pins listed as “A” on the secondary side of the motherboard and the 170 “B” pins on the primary side. Verify that pins A1 and B1 are toward the back I/O shield side of the motherboard.

PCI Signals

Generally ensure that all AD and control signals are terminated with a series resistor near the connector on the riser. A notable exception is that PCI_PM# needs to be pulled up on the motherboard. Refer to sections 2.1.1 and 2.1.2 for details on PCI simulation results.

— PCI Interrupts—Ensure that these signals have a termination/pullup resistor.

— PCI Clocks—For single I/O device support, use PCICLK0; for two devices, use PCICLK0 and PCICLK1; and so on. Take great care to minimize clock length and skew.

— REQ#/GNT#—For single riser master support, use REQ0#/GNT0#; for two devices, use REQ0#/GNT0# and REQ1#/GNT1#; and so on. Ensure that the appropriate pullup resistors are in place. Unused REQ#/GNT# pairs should be pulled-up.

— DEVSEL#—Ensure that DEVSEL# is pulled high on the riser with a weak pullup resistor.

— SER_IRQ—Route to the appropriate device. No pullup is required.

— AD, C/BE & remaining PCI signals—Ensure proper series termination.

— IDSEL Assignment—Begin assigning IDSEL signals from the upper address options (start by using IDESEL0).

— PCI_PM#—Should be routed to all PCI I/O slots. No pullup resistor should be in place.

— FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR# and LOCK#—Should be pulled high on the riser.

— REQ64#—Should be pulled high on the riser.

— ACK64#—Should be pulled high on the riser.

— SBO# and SDONE—Should be pulled up separately with an ~5KΩ resistor.

Power Signals

— 5VDC/3.3VDC/+12V/-12V/IEEE-1394//5VSB—Routed as plane or thick traces with the appropriate number of bulk and decoupling capacitors.

— PS_ON#—Route to on/off control on the power supply. The power supply provides the pullup.

— SOFT_ON/OFF#—If implemented as a front panel control signal, route to connector. The required debounce circuitry and appropriate pullup resistor to TTL levels reside on the motherboard.

— PWOK—Route to NLX connector and power supply connector.

ISA Signals

— All Signals—Route all signals directly to ISA connectors or ISA-based circuitry. All pullups are on motherboard.

IDE Signals

- Take great care to minimize trace lengths. All signals except IDEx_DASP are terminated (if required) on the motherboard with any appropriate pullups.
- IDEx_DASP—Ensure proper termination.

Floppy Signals

- All signals—Ensure that all signals requiring termination are properly terminated.

Miscellaneous Signals

- Reserved—Ensure that no traces are routed to this signal on the connector.
- Infrared—If IR port is implemented on front panel, ensure that signals are routed properly.
- PWRLED#—If there is LED support on the riser, ensure that a proper current limiting resistor is in place.
- LAN_LED#—If there is LED support on the riser, ensure that a proper current limiting resistor is in place.
- MSG_WTNG_LED#—If there is LED support on the riser, ensure that a proper current limiting resistor is in place
- FP_SLEEP—If front panel support is implemented for this signal, ensure it is routed correctly. The motherboard should have any required debounce and a weak pulldown resistor.
- FP_RST#—Route from the front panel support to signal on connector. To comply with the motherboard specification, the motherboard must provide any required pullup and debounce.
- MDM_WAKE #—A header is required for add-in modem cards. Route signal to the appropriate pin on the connector.
- LAN_WAKE—A header is required for add-in LAN cards. Route signal to the appropriate pin on the connector.
- USB data—Route from connector to any supported ports. If one port is supported, use USB1/3 signals on connector. To comply with the motherboard specification, the motherboard should contain any required series termination.
- USB_OC#—The thermistor located by the port should provide a pullup.
- PCSPKR_xx—If an 8 ohm speaker is supported, route it to the connector. If the speaker is mono, then the left signal is used by default.
- FAN_CTL—Ensure that a weak pullup to +12V exists on this signal. Route from headers to pin on connectors.
- TAMP_DET#—Route from the tamper detection switch to pin on connector.
- SDA/SCL—Wire from devices that utilize this bus to the connector, or leave it unconnected.

4. Motherboard Design Suggestions

The following sections discuss specific issues with designing motherboards to comply with the NLX specification.

4.1 PCI Bus Design

The PCI bus on the motherboard was simulated in significant detail. See sections 2.1.1 and 2.1.2 for detailed results. As a general rule, the PCI bus should be routed with extreme care to keep line lengths and skews to a minimum. PCI bus termination should comply with the current PCI specifications.

4.2 ISA Bus Design

Because all terminating resistors are on the motherboard, the motherboard designer should ensure that all appropriate signals are properly terminated.

4.3 IDE Bus Design

All terminating resistors except those needed for IDEA_DSP and IDEB_DSP are on the motherboard. These terminating resistors should be located as close as possible to the IDE controller. Series terminating resistors should be on the order of 33 ohms.

4.4 Floppy Bus Design

No special care is needed other than standard routing practices.

4.5 Motherboard Power Design

NOTE

A problem has been seen with VBAT shorting to ground when NLX motherboards are inserted or deinserted from riser cards. This shorting ultimately causes CMOS to be cleared. To prevent this, the NLX motherboard designer should place a resistor in series with the VBAT signal to the riser. This will limit the voltage drop to the CMOS device. Figure 15 shows an implementation.

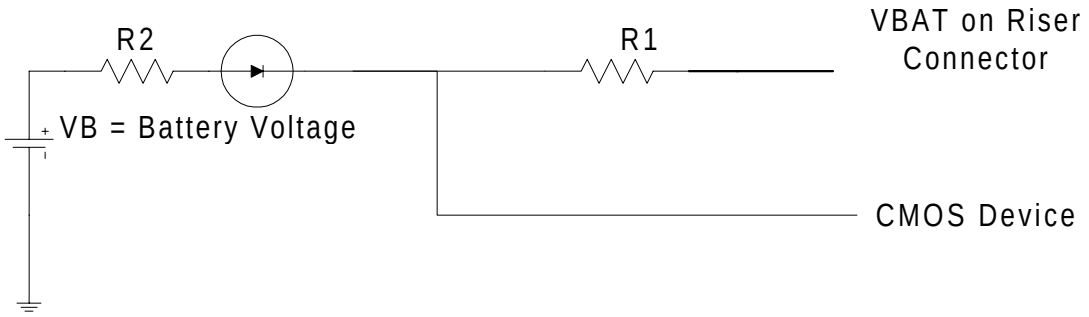


Figure 15: VBAT Circuitry

In this particular implementation, the voltage to the CMOS device never drops below VB(R1/(R1 + R2)) - 0.7V, where 0.7 is the voltage drop across the protective diode. R1 and R2 are system-specific and should be chosen to correspond to the minimum voltage required by the CMOS device and should be small enough not to prohibitively limit the current to the riser.

— VCC and VCC3—The appropriate number of bulk and decoupling capacitors is required to adequately support system requirements. The bulk capacitors should be low in ESR, and 22 uF or greater. The number needed is system-specific. The bulk capacitors should be placed where necessary for supporting circuitry that consumes large amounts of power on the motherboard. The decoupling capacitors should be in the range of 0.1 uF and placed judiciously about the motherboard. In addition, there should be an adequate number of stitching capacitors linking the VCC and VCC3 power planes where signals are required to cross the two planes.

— +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.

— PS_ON#—This signal should be routed from the motherboard power control circuitry to the 340-pin connector to allow the motherboard the ability to cycle power in the system. No other special care should be needed

— SOFT_ON/OFF#—Route from the NLX connector to the power control circuitry on the motherboard. No other special care should be needed.

— PWOK—Use this signal as needed to bring up the system in a controlled and orderly manner.

4.6 Motherboard Miscellaneous and Front Panel Signal Design

Most of the complexity of implementing front panel signals is referred to the riser. Specific issues involving the motherboard are dealt with in the following sections.

4.6.1 NLX Motherboard USB Design

The motherboard designer needs to understand how USB will be supported in the system. If the USB controller supports two USB ports, then the motherboard designer should implement one port out of the back panel and route the second port to the NLX connector for possible front panel support. If no ports are being supported out the back panel, then the motherboard designer should

route both ports to the NLX connector. The motherboard should provide overcurrent protection only for those ports that are directly supported. Overcurrent protection should not be implemented for ports that are supported on the riser.

4.6.2 Fan Control

A circuit similar to that shown in Figure 16 may be used on the motherboard to create a minimum function FAN_CTL signal. This signal will result in a fan control output level of either 8 volt or 11.6 volts, depending on the level of the GPIO input. This level of control will allow the fan speed to vary from full on to an intermediate level but will never turn the fan off.

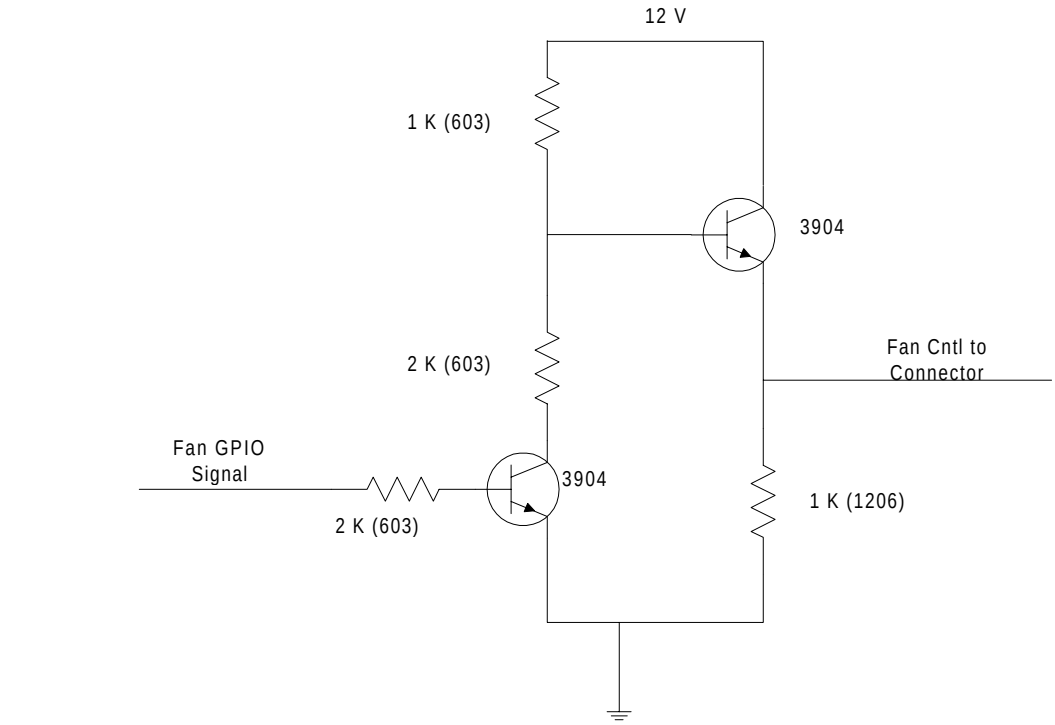


Figure 16: Motherboard NLX Fan Control Circuitry

4.6.3 Fan Tach

Special care should be implemented on monitoring the fan tach signals from the riser. These signals may or may not be utilized on the riser, and the motherboard will have no way to distinguish between the signal not being utilized on the riser and the fan malfunctioning. Therefore, it is highly recommended that the motherboard implement power management software that will let the user determine whether or not individual fan tach signals on the NLX connector interface are monitored by the motherboard.

4.6.4 Other Miscellaneous Signals

All other miscellaneous signals are straightforward with regard to the motherboard implementation. What the motherboard does with input signals from the riser is motherboard-specific and is beyond the scope of this document. Outputs are also motherboard-specific, and

what the riser does with these signals is outside the control of the motherboard. For example, when the system enters sleep state, the motherboard should drive the PWRLED signal high. This may cause the riser to blink a light or turn a dual-color light to the complementary color. As another example, when a message has been received in the system, the motherboard needs to drive the MSG_WTNG# signal active; what the riser does with the signal is totally transparent to the motherboard. It could drive a single color LED, or blink a single color LED, or blink a dual color LED, etc.

4.7 NLX Motherboard Checklist

This section provides an informal checklist of suggestions about the motherboard electrical design. The checklist is meant for reference only and is not intended to be comprehensive.

NOTE

It is strongly recommended that the NLX specification be reviewed in sufficient detail that the designer is confident the design complies with the specification.

Motherboard Mechanical/Placement Requirements

- Ensure that board size is between 8"×10" and 9"×13.6".
- Ensure that mounting holes are placed in accordance with the NLX specification.
- Ensure that primary side plated keep-out areas are centered around the required four mounting holes and are properly grounded (keep-out area A).
- Ensure that secondary side keep-out areas are centered around required mounting holes (trace and component keep-out) and those for rail bumpers (component keep-out).
- Recommended: Secondary side component keep-out area B for rail-less mounting.
- Optional: EMI clip sites can be placed in areas specified in the NLX specification.
- Ensure the pin card edge connector is placed and structured as shown in the NLX specification.
- Ensure that the notched area is implemented to allow for supplemental riser connector.
- If an A.G.P. connector is supported (9" boards only), it must be placed as shown in the NLX specification.
- Ensure that the motherboard primary side keep-out zones are as shown in the NLX specification.
- Ensure that the motherboard secondary side keep-out zones are as shown in the NLX specification.
- Ensure that height restrictions on the rear I/O panel are not violated.

Motherboard NLX Card Edge Signal Issues

- Ensure the 1mm pitch connector setup is as listed in the tables in the NLX specification. The 170 pins listed as “A” are on the secondary side of the motherboard and the 170 “B” pins are on the primary side. Verify that pins A1 and B1 are toward the back I/O shield side of the motherboard.

PCI Signals

PCI signals are generally terminated on the riser. A notable exception is that PCI_PM# needs to be pulled up on the motherboard. Some point-to-point signals should not be routed to the riser if used on the motherboard. If followed, the recommendations about resource allocation can alleviate some interoperability issues.

— PCI Interrupts—Route to riser, allowing for termination/pullups on the riser. If possible, check specific riser card implementation.

— PCI Clocks—Route to edge connector to support any riser-based PCI devices or slots. For single riser device support, route to PCICLK0; for two devices, route to PCICLK0 and PCICLK1; and so on. Appropriate termination should reside on the motherboard for riser clocks. Take great care to minimize clock length and skew

— REQ#/GNT#—Route to edge connector to support any riser-based PCI masters. For single riser master support, use REQ0#/GNT0#; for two devices, use REQ0#/GNT0# and REQ1#/GNT1#; and so on. Appropriate pullup resistors will reside on the riser. Note that REQ#/GNT# pairs for motherboard-based PCI devices should not be routed to the riser and therefore should be terminated on the motherboard.

— SER_IRQ—If supported, provide pullup and route to the riser.

— AD, C/BE & remaining PCI signals—Route to the riser. Termination resides on the riser. If possible, check specific riser card implementation.

— IDSEL Assignment—Ensure the assigning of IDSEL signals from the lower options (start by using IDESEL0).

— PCI_PM#—This signal should be routed to the device that can generate a proper SMI type of condition. Ensure that an appropriate pullup is in place.

Power Signals

— VBAT—Ensure that a series resistor is place between the source and the riser.

— 5VDC/3.3VDC/+12V/-12V/IEEE-1394/Powergood/5VSB—Ensure signals are routed as a plane or thick traces.

— PS_ON#—Intended to control power supply on the riser. This signal is open drain. The power supply provides the pullup.

— SOFT_ON/OFF#—Ensure that the proper debounce circuitry and appropriate pullup resistor to TTL levels are in place.

— PWOK—Utilize this signal as needed to ensure proper initialization of motherboard circuitry.

ISA Signals

— Ensure that all ISA signals are properly terminated with any appropriate pullups.

IDE Signals

— All Signals except IDEx_DASP—Should be terminated (if required) on the motherboard with any appropriate pullup resistors. Take great care to minimize trace lengths.

— IDEx_DASP—Should be terminated on the riser card. If possible, check specific riser card implementation.

Floppy Signals

— All floppy signals should be terminated (if required) on the riser with appropriate pullup resistors. If possible, check specific riser card implementation.

Miscellaneous Signals

— Reserved—Not to be driven or routed.

— Infrared—Should be routed if desired.

— PWRLED#—Ensure that signal is properly routed to the riser. The riser should have a current limiting resistor.

— LAN_LED#—Ensure that signal is properly routed to riser. The riser should have a current-limiting resistor.

— MSG_WTNG_LED#—Ensure that signal is properly routed to the riser. The riser should have a current-limiting resistor.

— FP_SLEEP—Ensure that proper pullup and debounce circuitry are in place.

— FP_RST#—Ensure that proper pullup and debounce circuitry are in place.

— MDM_WAKE #—Ensure that this signal, if utilized, is routed to a schmitt trigger input buffer.

— LAN_WAKE—Ensure that this signal, if utilized, stays low when power is applied to the system.

— USB data—If one port on riser is supported, route to USB1/3 signal-on connector. Ensure that proper series termination is in place.

— USB_OC#—Thermistor located by the port should provide the pullup.

— PCSPKR_xx—Meant to drive an 8 ohm speaker on the riser. The left signal is used by default to drive mono audio.

— FAN_TACHx—These signals run from 0V to +12V. The motherboard must provide any voltage conversion for 5V or 3.3V devices.

— FAN_CTL—Voltage provided should be between 0V and 12V. The riser should have a weak pullup to 12V.

— TAMP_DET#—Open drain signal from the riser. Implementation of pullup to VBAT or 5VSB needs to be decided upon.

— SDA/SCL—Wire to riser. Bidirectional SM Bus. Ensure pullup resistors are in place.

5. Electrical Implementation of AGP

A main issue that must be addressed in implementing AGP on NLX platforms is the skew between traces during synchronous (2X Mode) operations. The skew is affected by such parameters as line length mismatch, capacitive loading variations, settling time, and crosstalk. Figure 17 shows the components of skew. As shown, settling time and crosstalk have the largest effects on skew; these interact with each other and the other parameters to compound the problems.

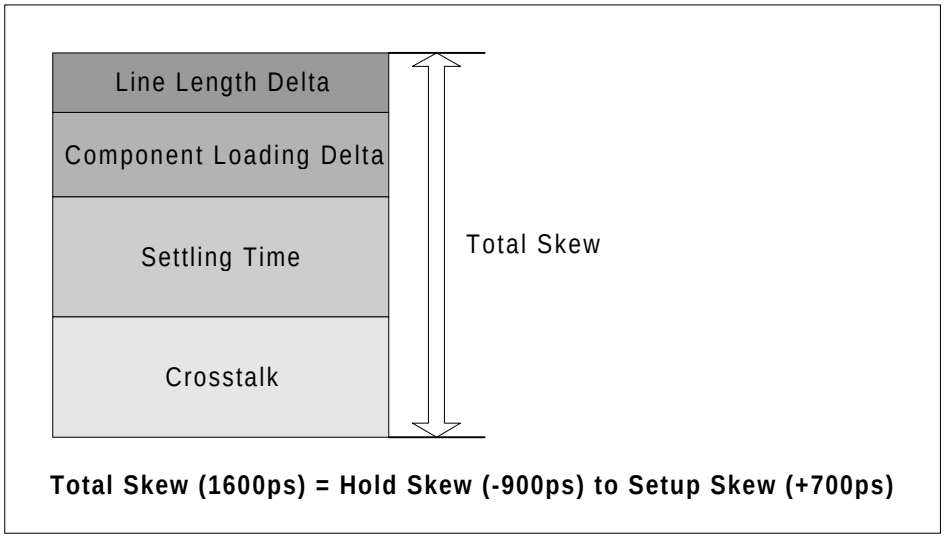


Figure 17: Skew Components

5.1 Simulation Results

The simulation results presented are for a specific motherboard and chipset combination. Therefore, motherboard OEMs are encouraged to perform their own independent simulations that will help guide the choice of and layout of the components. Table 6 summarizes the recommendations resulting from our simulation studies.

Table 6: Motherboard Recommendations for AGP

Width:Space	Zo	Trace	Line length	Line length matching
1:1	50Ω to 85Ω	Data / Strobe	1.0in < line length < 4.5in	-0.5in, strobe longest trace
1:2	50Ω to 85Ω	Data / Strobe	1.0in < line length < 9.5in	-0.5in, strobe longest trace

The first column of Table 6 signifies that the maximum line length depends on the routing rules on the motherboard. The width:space designation refers to the width of the trace in relation to the distances between traces. Because crosstalk is a key contributor to skew and crosstalk is decreased with increasing distance between traces, then it is no surprise that you can achieve longer line lengths with larger ratios.

Table 7 shows the constraints imposed on the clock and control signals of the AGP bus. Because some of the control signals require pullup resistors, the stub to these resistors should be tightly controlled. The clock lines on the motherboard strictly depend on the clock driver that is being used and the motherboard trace topology, so specific simulation needs to be done on these signals.

Table 7: Control and Clock Signal Recommendations

Width:Space	Board	Trace	Line Length	Pullup Stub Length
1:1	Motherboard	Control Signals	1.0in < line length < 8.5in	< 0.1in
1:2	Motherboard	Control Signals	1.0in < line length < 10.0in	< 0.1in
1:4 to strobe	Motherboard	Clock		

In multilayer motherboards, take care to ensure that all signals are routed as a group. This implies that the group is collectively routed as either microstrip or stripline but not combined. This is necessary because traces routed on the external layer (microstrip) have different propagation delays than traces routed on internal layers (stripline).

6. EMI Containment on NLX Systems

EMI containment is becoming increasingly more difficult in PC systems, and NLX PC systems are no different. NLX systems provide the motherboard engineer the benefit of several strips in the chassis assured of good electrical contact to chassis ground. This allows the designer the flexibility of addressing EMI hotspots by providing ground clips to the strip.

Figure 18 shows the EMI clip location areas; this figure is repeated here from NLX motherboard specification. The three clip location areas are placed strategically along the length of the board and extend approximately across the width. The following is a list of suggestions to help designers limit the amount of EMI in their designs.

- Use the widest trace possible for all routes. At a minimum, use 6 mils for noncritical nets and 8 mils for clock traces.
- Separate the signal traces into similar categories, and route similar signal types together.
- Route high speed (>10Mhz) signals on the bottom or inner layers whenever possible.
- Route high speed signals using a minimum number of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° bends or an arc instead of making a single 90° turn. This reduces the reflections on the signal.
- Maximize spacing between adjacent traces. This reduces crosstalk.
- Keep traces at least 100 mils away from the edge of the ground plane. This helps prevent the signal from coupling into adjacent wires, boards, etc.
- It is recommended to route all traces over a continuous ground plane, with no interruptions (i.e., do not cross any plane splits) whenever it is possible

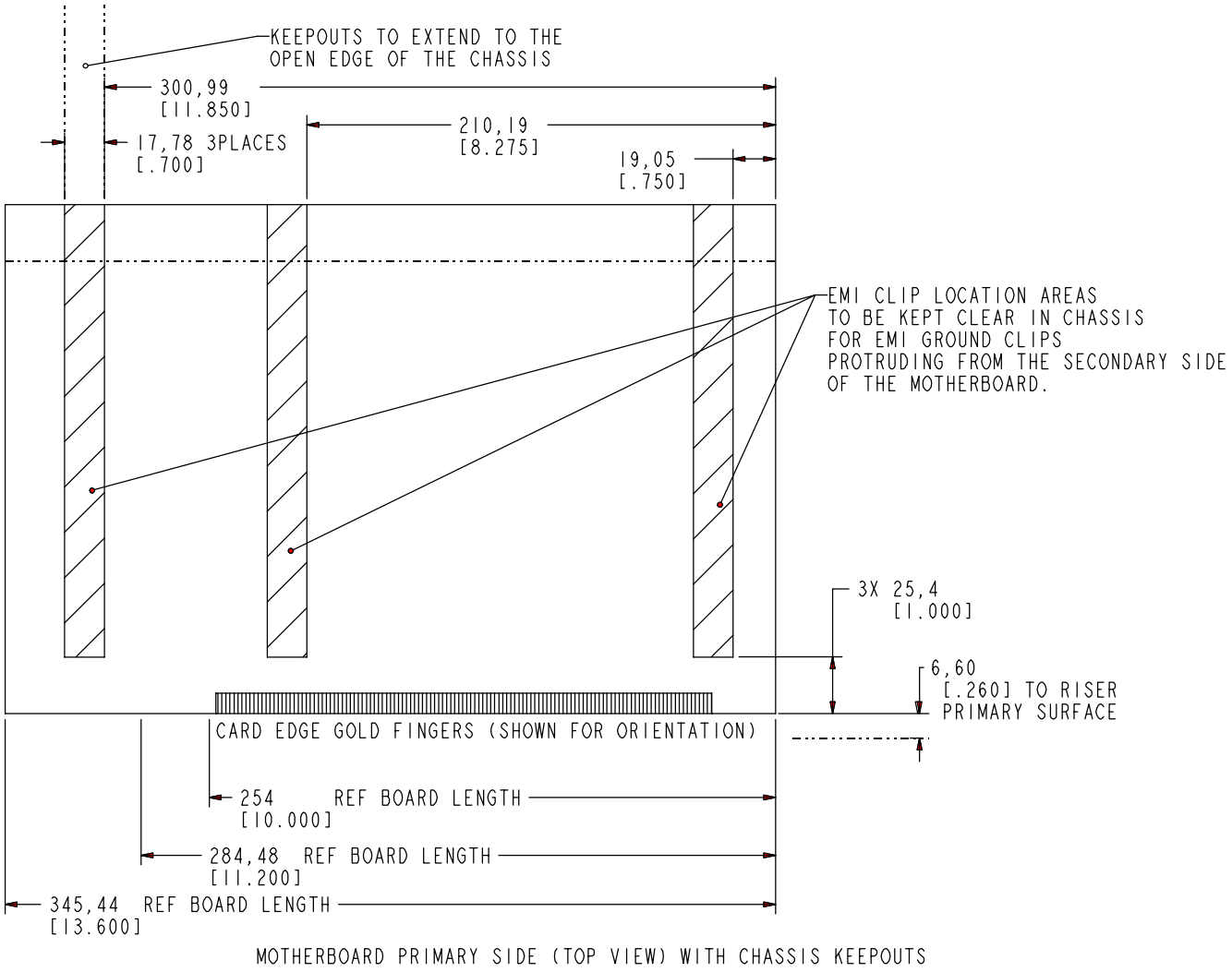


Figure 18: EMI Clip Location Areas